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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/584,395	06/23/2006	Keiko Fukuda	XA-10578	9000

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EXAMINER	
COLE, BRANDON S	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/584,395	FUKUDA ET AL.	
	Examiner	Art Unit	
	BRANDON S. COLE	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 13th 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5,6,8,9 and 16* is/are rejected.

7)☒ Claim(s) *7,10-15, 17, and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *June 23rd 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's amendment filed on 7/02/2008 has been entered in the case. After further consideration a new interpretation is now relied upon examiner to reject the claims. Therefore, this action is non-final.

Claim Objections

2. Claims 1-18 are objected to because of the following informalities: The claimed first, second, third, and fourth resistances should each be replaced with "resistive element." For example, "…a first resistance" should be replaced with "….a first resistive element." Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 3 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Brokaw (US 3,887,863) in view of Cheng (US 5,132,556).

As to claim 1, Brokaw figure 1 shows a voltage generating circuit comprising: a first transistor (Q2) which allows a first current to flow in an emitter thereof; a second transistor (Q1) which allows a second current having a current density larger than a current density of the emitter of the first transistor to flow in an emitter thereof; a first resistance (R2) which is provided between the emitter of the first transistor and the emitter of the second transistor; a second resistance which is provided between the emitter of the second transistor and a ground potential of the voltage generating circuit; a third resistance which is provided between a collector of the first transistor and a power source voltage (R_{L2}); a fourth resistance (R_{L1}) which is provided between a collector of the second transistor and the power source voltage; and a differential amplifier circuit (28) having which forms an output voltage upon receiving a collector voltage of the first transistor and a collector voltage of the second transistor, and, which supplies the output voltage to bases of the first transistor and the second transistor in common.

Brokaw fails to show that the differential amplifier having a CMOS constitution and that the wherein the first transistor and the second transistor are constituted by making use of a semiconductor region formed in a CMOS process associated with of a CMOS circuit which constitutes the differential amplifier circuit..

However, Cheng figure 1 shows a differential amplifier having a CMOS constitution and that the wherein the first transistor (6) and the second transistor (8) are

constituted by making use of a semiconductor region formed in a CMOS process associated with of a CMOS circuit which constitutes the differential amplifier circuit. Cheng teaches in column 1, lines 34 – 39 that figure 1 is an CMOS integrated circuit and the first (6) and second transistors (8) are parasitic NPN transistors, each of which uses the IC substrate for its collector, a P-well for its base, and an N-type drain/source region for its emitter. Cheng teaches in column 2, lines 14 – 15 that the amplifier (26) has a CMOS constitution.

Therefore, it would have been obvious for one having ordinary skill in the art, at the time of the invention, to replace Brokaw's differential amplifier and both transistors with Cheng's CMOS differential amplifier and transistors that are available from a CMOS process for the purpose of generate a voltage with a positive temperature coefficient having the same magnitude as the negative temperature coefficient of V_{BE}; then to add V_{BE} to the generated voltage to cancel the temperature dependency.

As to claim 2, Brokaw figure 1 shows voltage generating circuit wherein the third resistance (R_{L2}) and the fourth resistance (R_{L1}) are configured to possess a same resistance value.

As to claim 3, Brokaw figure 1 a voltage generating circuit wherein an emitter area of the first transistor (Q2) is set larger than an emitter area of the second transistor (Q1).

Claim 5 has similar limitations as claim 1. Therefore the claims are rejected for the same reasons.

6. Claims 6, 8, 9, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brokaw (US 3,887,863) in view of Cheng (Us 5,132,556), as applied to claim 5, in further view of Yasuoka (US 5,017,996).

Cheng figure 4 shows a CMOS process circuit is realized including a lateral npn transistor.

Brokaw and Cheng fail to show that the CMOS circuit having a second conductive-type well region and a first conductive-type well region formed on a first conductive-type semiconductor substrate a first conductive-type MOSFET formed on the second conductive-type well region, and a second conductive-type MOSFET formed on the first conductive-type well region ,wherein each of the first transistor and the second transistor of the reference voltage generating circuit formed of a bipolar transistor having a lateral structure with collector, emitter, and base portions being constituted by diffusion layers formed on respective portions of a first conductive-type well arrangement, the diffusion layers of the collector and emitter portions being formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET.

However, Yasuoka figure 10 shows CMOS circuit having a second conductive-type well region (n-well) and a first conductive-type well region (p-well) formed on a first conductive-type semiconductor substrate (P-sub), a first conductive-type MOSFET (p-

channel) formed on the second conductive-type well region, and a second conductive-type MOSFET (n-channel) formed on the first conductive-type well region, a lateral bipolar transistor structure with collector, emitter, and base portions being constituted by diffusion layers formed on respective portions of a first conductive-type well arrangement, the diffusion layers of the collector and emitter portions being formed in a step for forming source and drain diffusion layers of the second conductive-type MOSFET. Yasuoka teaches in column 2, lines 36 – 38 that the CMOS IC having an n-channel MOSFET formed in a surface region of a p-well provided in the substrate is formed. Yasuoka teaches in column 8, lines 39 – 42 it is possible to form an n-well in the n-epitaxial layer in which the p-channel MOSFET is formed. Yasuoka teaches in column 5, lines 62-65 that the source and drain of the N-channel MOS FET device is formed by a known self-alignment technique in a surface region of the p-well.

Therefore it would have been obvious for one having ordinary skill in the art, to replace Cheng's CMOS process with Yasuoka's CMOS process for the purpose of providing the BiMOS IC with an improved breakdown voltage without drastically changing the production process.

Claim 8 has similar limitations as claim 6. Therefore the claim is rejected for the same reasons.

As to claim 9, Cheng figure 4 shows a semiconductor integrated circuit device wherein wherein the power source voltage supplied from the second external terminal is

positive (VCC). Cheng teaches in column 5, lines 34 – 35 that the inventions CMOS process and other CMOS process are suitable for realizing transistors.

Cheng fails to show that the first conductive-type is a p-type and the second conducive-type is an n-type.

However, Yasuoka shows that the first conductive-type is a p-type and the second conducive-type is an n-type. Yasuoka teaches in column 2, lines 36 – 38 that the CMOS IC having an n-channel MOSFET formed in a surface region of a p-well provided in the substrate is formed. Yasuoka teaches in column 8, lines 39 – 42 it is possible to form an n-well in the n_--epitaxial layer in which the p-channel MOSFET is formed.

Therefore it would have been obvious for one having ordinary skill in the art, to replace Cheng's CMOS process with Yasuoka's CMOS process for the same reasons as above.

Claim 16 has similar limitations as claim 9. Therefore the claim is rejected for the same reasons.

Response to Arguments

7. Applicant's arguments with respect to claims 1-3, 5, 6, 8, 9 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

8. Claims 7, 10-15, 17 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. COLE whose telephone number is (571)270-5075. The examiner can normally be reached on Mon - Fri 7:30-5:00 EST (Alternate Friday's Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on (571) 272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Long Nguyen/
Primary Examiner, Art Unit 2816

/Brandon S Cole/
Examiner, Art Unit 2816